AP

MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP7058107
Publication date: 1995-03-03
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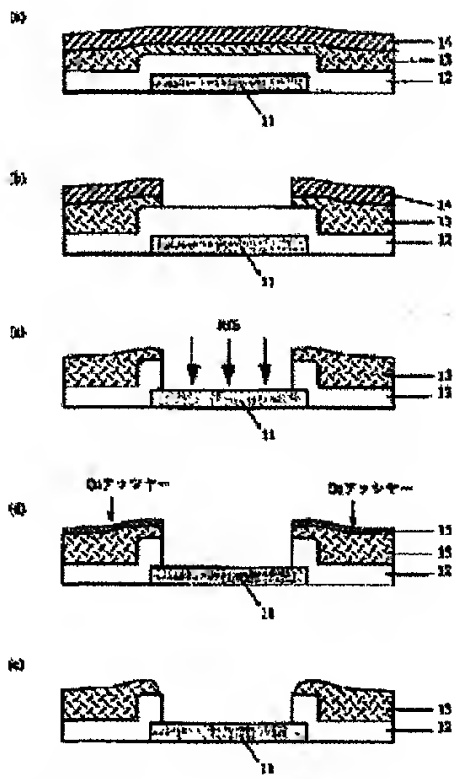
Classification:
- International: ***H01L21/302; H01L21/3065; H01L21/312; H01L21/3205; H01L21/3213; H01L23/52;*** H01L21/02; H01L23/52; (IPC1-7): H01L21/3205; H01L21/3065; H01L21/312; H01L21/3213
- European:
Application number: JP19930203810 19930818
Priority number(s): JP19930203810 19930818

Abstract of **JP7058107**

PURPOSE:To remove fluorine remaining on the surface of a polyimide film nearly perfectly by performing dry etching of an inorganic insulating film by RIE using the polyimide film as a mask, and by removing the surface of the polyimide film by a given quantity after that. CONSTITUTION:An opening is formed in an inorganic insulating film 12 by dry etching by RIE, using a polyimide film 13 having a specified holed part as a mask. After the surface layer of the polyimide film 13 of a thickness of about 2,000 angstrom is removed by an O2 plasma asher method, as a processing of the polyimide surface layer after the dry etching I.e., a fluorine remaining layer 15, washing by water and heat treatment are performed, and a laminated passivation film, composed of the inorganic insulating film 12 and the polyimide film 13 not having a fluorine remaining layer 15 in the polyimide film 13, is completed. As a result of this, it becomes possible to prevent the corrosion of pads and wirings even if water enters molding resin.



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Publication info: JP7058107 A - 1995-03-03

Data supplied from the ***esp@cenet*** database - Worldwide

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平7－58107

(43)公開日　平成7年(1995)3月3日

(51)Int.Cl.[6]	識別記号	庁内整理番号	FI		技術表示箇所
H01L 21/3205					
21/3065					
21/312	M	7352－4M			
		8826－4M	H01L 21/88	T	
			21/302	N	

審査請求　未請求　請求項の数2　ＯＬ　（全 5 頁）　最終頁に続く

(21)出願番号　特願平5－203810

(22)出願日　平成5年(1993)8月18日

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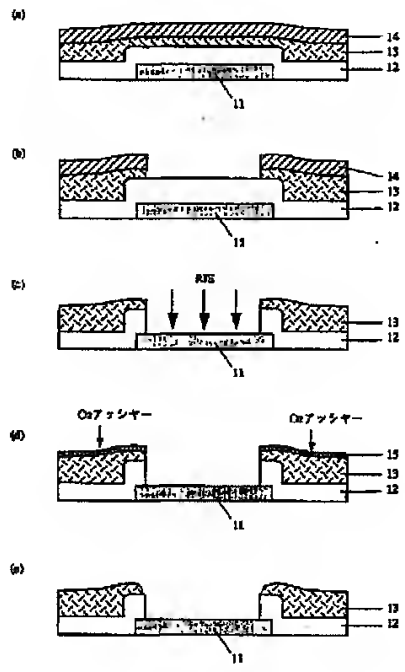
(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【構成】ポリイミド膜１３と無機絶縁膜１２とからなる積層パッシベーション膜形成プロセスにおいて、半導体基板上に所定のパターンを有する金属配線１１上にパッシベーション用の無機絶縁膜１２を形成する工程と、ポリイミド膜１３を形成する工程とにより積層パッシベーション膜を形成し、ポリイミド膜１３を開孔する工程と、ポリイミド膜１３をマスクにして無機絶縁膜１２を開孔する工程により、積層パッシベーション膜の所定の位置に開口部を形成した後、ポリイミド膜１３の表面層を一定量除去する工程を具備した事を特徴としている。

【効果】本発明による半導体装置の製造方法によれば、モールド樹脂中に水分が侵入しても、パッドや配線のコロージョンが発生しにくく、かつ、モールド樹脂との密着性の良好な半導体装置の製造方法を提供することが出来る。



【特許請求の範囲】

【請求項１】　半導体基板上に形成された金属配線上に無機絶縁膜を形成する工程と、
前記無機絶縁膜上にポリイミド膜を形成する工程と、
前記ポリイミド膜上にフォトレジストを形成する工程と、
前記フォトレジストを所定の形状に形成した後、これをマスクとして前記ポリイミド膜にエッチングにて所定の開口部を設ける工程と、
前記フォトレジストを除去する工程と、
前記ポリイミド膜をマスクにして前記無機絶縁膜にＲＩＥによるドライエッチングを施す工程と、
前記ポリイミド膜の表面層を一定量除去する工程とから構成される積層パッシベーション膜形成工程を有することを特徴とする半導体装置の製造方法。

【請求項２】　前記ポリイミド膜の表面層を一定量除去する工程が、O_2 プラズマアッシャー法により行われることを特徴とする請求項１記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体装置とその製造方法に関し、特に、ポリイミド膜と無機絶縁膜層からなる積層パッシベーション膜において、この無機絶縁膜層に開口部を形成する工程に関する。

【０００２】

【従来の技術】従来の、ポリイミド膜と無機絶縁膜層とからなる積層パッシベーション膜の開口部加工工程の一例について、図３及び図４を参照しながら説明する。まず、半導体基板上に形成された所定のパターンを有する金属配線３１上に、無機絶縁膜３２、低温ベークのみ行なったポリイミド膜３３を順に形成した後、ポジ型フォトレジスト３４を塗布する（図３（ａ））。続いて露光、現像を行ない、ポリイミド膜３３をポジ型フォトレジスト３４の現像と同時にエッチングし、このポリイミド膜３３に所定の開口部を設ける（図３（ｂ））。有機溶剤によりポジ型フォトレジスト３４を選択的に剥離した後、所定の熱処理を行ない、ポリイミド膜３３をイミド化させる。次にこのポリイミド膜３３をマスクにして、通常のReactive Ion Etching（以下、ＲＩＥと略記する）法により無機絶縁膜３２に開孔した後（図３（ｃ））、水洗、ポリイミド再熱処理を行ない、ポリイミド膜と無機絶縁膜から構成される積層パッシベーション膜の開口部形成を完了する（図３（ｄ））。

【０００３】上述の様に、従来のポリイミド膜と無機絶縁膜の積層パッシベーション膜の開口部形成方法では、開口部を加工する際にポリイミド膜をマスクにして、ＲＩＥ等のドライエッチング法で無機絶縁膜の開孔を行なっている。ドライエッチングとは、真空中に反応性ガスを注入して化学反応によりエッチングする方法であり、一般に、シリコン酸化膜（不純物ドーピング膜を含む）やシリコン窒化膜等のドライエッチングには、フッ素元素を含むガスが使用されている。この場合の一般的な化学反応式について次に示す。尚、F^* は、化学的に極めて活発な、ラジカル状態のフッ素を示す。

【０００４】

$SiO_2 + F^* \rightarrow SiF_4 + O_2$

$Si_3N_4 + F^* \rightarrow SiF_4 + N_2$

しかし、このエッチングガスがプラズマ中で不飽和モノマーを生成してしまい、このエッチング残渣の影響を受けて、図３（ｄ）に示すようにポリイミド膜の表面層に高濃度のフッ素残留層３５が形成されてしまう。

【０００５】図４は従来例におけるポリイミド膜における元素別の濃度を深さ分布として表したものである。横軸はポリイミド膜における深さを、縦軸は各元素の濃度を示している。このグラフ（Ｆ－３）に示される様に、表面近傍においてフッ素の濃度が非常に高くなっている。この高濃度のフッ素残留層３５は、再度の熱処理（３５０℃－６０分）による後処理では、ほとんど除去されない。このような、フッ素残留層３５の存在により、以下のような問題点が生じている。

【０００６】まず一つは、エッチング後に大気中の水分に接触して反応したり、モールド樹脂中に侵入した水分とフッ素残留層のフッ素が反応してフッ酸が形成されて、パッド部等の腐食による配線コロージョンが発生してしまうという点である。配線の腐食は素子の歩留りを低下させるばかりでなく、配線の信頼性寿命を著しく低下させ、素子の寿命を低下させる原因にもなる。Pressure and Cooker Test（高温・高圧スチームテスト。信頼性評価の項目の一つ。以下、ＰＣＴと略記する。）による信頼性寿命は８０時間～１５０時間と短く、また、バラツキも大きくなってしまうという点である。

【０００７】また二つ目として、フッ素残留層の存在により、モールド樹脂との密着性が低下し、Temperature Cycling Test（信頼性評価の項目の一つ。以下、ＴＣＴと略記する。）によると２００～４００サイクルでモールドとの剥れが生じる。この為に外部からの水分の侵入が容易になり、これに起因してフッ酸形成による配線コロージョンの問題等の発生も助長されてしまうので、更に信頼性レベルの低下が生じることになっているという点である。

【０００８】

【発明が解決しようとする課題】上述のように、従来の半導体装置の製造方法では、ポリイミド膜と無機絶縁膜から成る積層パッシベーション膜に開口部を形成する際のドライエッチングに用いるフッ素含有ガスにより、ポリイミド膜表面層に高濃度のフッ素残留層が形成されてしまい、この影響で、モールド樹脂により封止した後、パッド部等の配線コロージョンが発生したり、モールド樹脂剥離が生じて、信頼性の低下を招くという問題があ

った。

【０００９】本発明では、上述した問題点を解決する為に、ドライエッチング後、ポリイミド膜表面に残留したフッ素をほぼ完全に除去し、信頼性を向上させた半導体装置とその製造方法を提供することを目的とする。

【００１０】

【課題を解決するための手段】上記目的を解決するために、本発明では、半導体基板上に形成された金属配線上に無機絶縁膜を形成する工程と、前記無機絶縁膜上にポリイミド膜を形成する工程と、前記ポリイミド膜上にフォトレジストを形成する工程と、前記フォトレジストを所定の形状に形成した後、これをマスクとして前記ポリイミド膜にエッチングにて所定の開口部を設ける工程と、前記フォトレジストを除去する工程と、前記ポリイミド膜をマスクにして前記無機絶縁膜にＲＩＥによるドライエッチングを施す工程と、前記ポリイミド膜の表面層を一定量除去する工程とから構成される積層パッシベーション膜形成工程を有することを特徴とする半導体装置の製造方法を提供する。また、前記ポリイミド膜の表面層を一定量除去する工程が、O_2 プラズマアッシャー法によって行われることを特徴とする半導体装置の製造方法を提供する。

【００１１】

【作用】上述のように構成された本発明の半導体装置とその製造方法によれば、ドライエッチング後、ポリイミド膜表面に残留したフッ素をほぼ完全に除去することにより、パッドコロージョンの発生やモールド樹脂との密着不良を抑制し、信頼性を向上させることが可能となる。

【００１２】

【実施例】本発明の一実施例について、図１及び図２を参照しながら説明する。図１（ａ）～図１（ｅ）は、本発明の一実施例における半導体装置の製造工程を示す断面図である。以下に、本実施例の製造工程について説明する。

【００１３】まず、所定のパターンを有した、例えばＡｌ－Ｓｉからなる金属配線１１（厚さ：約１．０μｍ）上に、通常のプラズマＣＶＤ法により無機絶縁膜１２として１μｍ厚のＰ－ＳｉＯ膜を形成し、この無機絶縁膜１２のＰ－ＳｉＯ膜上にポリイミド膜１３を約３．２μｍ（４０００rpm －６０秒）塗布をする。更に１４０℃（５分）のベーク後、ポジ型フォトレジスト１４を約２．５μｍ（４０００rpm －３０秒）塗布し、１１０℃（６０秒）のベークを行う（図１（ａ））。

【００１４】次に、所定のパターンを有するマスクを用い、露光後、アルカリ系現像液により、ポジ型フォトレジスト１４の現像とポリイミド膜１３のエッチングを連続して行ない、ポリイミド膜１３に所定のパターンを形成する（図１（ｂ））。

【００１５】続いて、有機溶剤により、ポジ型フォトレジスト１４を選択的に除去した後、所定の手順でベーク（（２５０℃－３０分）＋（３５０℃－４０分））を行ない、ポリイミド膜１３のイミド化を完了させる。この後所定の開孔部をもつ、ポリイミド膜１３をマスクにこの無機絶縁膜１２の開孔を、通常のＲＩＥによるドライエッチングで行う（図１（ｃ））。

【００１６】更に、ドライエッチング後のポリイミド表面層、つまりフッ素残留層１５の処理として、O_2 プラズマアッシャー法でポリイミド膜１３表面層の２０００オングストローム程を除去した後（図１（ｄ））、水洗い（１０分）と、熱処理（３５０℃－６０分）を行い、ポリイミド膜１３中にフッ素残留層１５の無い、ポリイミド膜１３と無機絶縁膜１２とからなる積層パッシベーション膜を完成させる（図１（ｅ））。

【００１７】尚、実施例中では、ポリイミド表面層のフッ素残留層の処理としてO_2 プラズマアッシャー法を行なっているが、フッ素の再吸着のない化学的エッチング法であれば、O_2 プラズマアッシャー法に限らなくて良い。また、ポリイミド表面層の除去量として２０００オングストローム除去するとしたが、それ以下の除去量でもフッ素残留層を除去しきれるのならば勿論差支えないので、例えばこの実施例での分析の結果から考えるならば、少なくとも８００オングストローム以上除去すれば良いと考えられる。このポリイミド表面層の除去量については、対象の積層パッシベーション膜や、条件に応じて対応すれば良い。更に、例えば無機絶縁膜として用いたＰ－ＳｉＯ膜やその他の構成材料についても、適するものであれば他の材質でも差支えない。フォトレジストについても必ずしもポジ型である必要はなく，場合に応じて適するものを使用する。

【００１８】図２（ａ）及び（ｂ）はポリイミド膜における元素別の濃度を深さ分布として表したものである。横軸はポリイミド膜における深さを、縦軸は各元素の濃度を示している。図２（ａ）のグラフ（Ｆ－１）は、ポリイミド膜表面層処理後のポリイミド膜中残留フッ素の深さ分布を示す図であり、図２（ｂ）のグラフ（Ｆ－２）は、積層パッシベーション膜形成後にドライエッチングを実施していないサンプルにおけるフッ素の深さ分布を示した図であるが、例えば、前述の実施例のように、表面２０００オングストロームをO_2 プラズマアッシャー法で除去した場合、図２（ａ）に示す様に、ＲＩＥなどドライエッチングを実施していないサンプル図２（ｂ）と同様にフッ素は、ほとんど検出されないことが示される。

【００１９】以上の様に、上述のようなO_2 プラズマアッシャー法を施すと、ポリイミド表面のフッ素残留層がほぼ完全に除去できることから、以下の利点がある。まず、モールド樹脂中に水分が侵入しても、フッ素が存在しない為、パッドや配線のコロージョンが発生しにくい。例えば、ＰＣＴによる信頼性寿命は、４００時間以

上と、従来の２．６～５倍に延びた値を得ることが出来る。

【００２０】また、フッ素残留層が存在しない為に、モールド樹脂との密着性が安定しており、ＴＣＴでは、１０００サイクルに達しても、モールドとの剥れが生じない。この為、外部からの水分の侵入が難しく、信頼性レベルの向上した半導体装置を得ることが出来る。

【００２１】

【発明の効果】本発明による半導体装置の製造方法によれば、モールド樹脂との密着性の良好であり、モールド樹脂中に水分が侵入しても、パッドや配線のコロージョンが発生しにくい半導体装置の製造方法を提供することが出来る。

【図面の簡単な説明】

【図１】（ａ）～（ｅ）は、本発明の一実施例における製造工程を示す断面図、

【図２】（ａ）はポリイミド膜表面層処理後のポリイミド膜中残留フッ素の深さ塗布を示す図、（ｂ）は積層パッシベーション膜形成後にドライエッチングを実施していないサンプルにおけるフッ素の深さ分布を示す図、

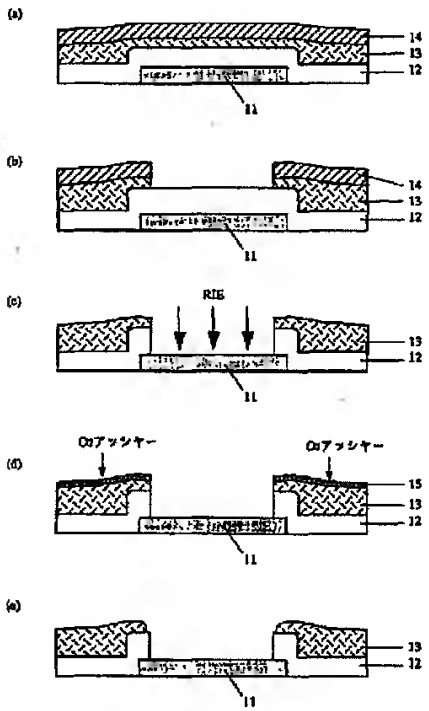
【図３】（ａ）～（ｄ）は従来例における製造工程を示す断面図、

【図４】ドライエッチング後のポリイミド膜中の残留フッ素の深さ分布を示す図。

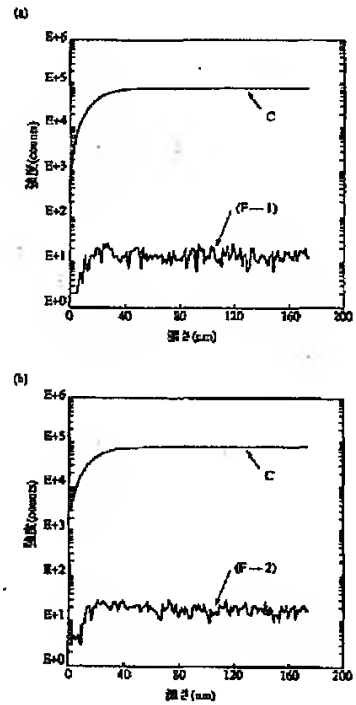
【符号の説明】

１１　金属配線
１２　無機絶縁膜
１３　ポリイミド膜
１４　ポジ型フォトレジスト
１５　フッ素残留層

【図１】



【図２】



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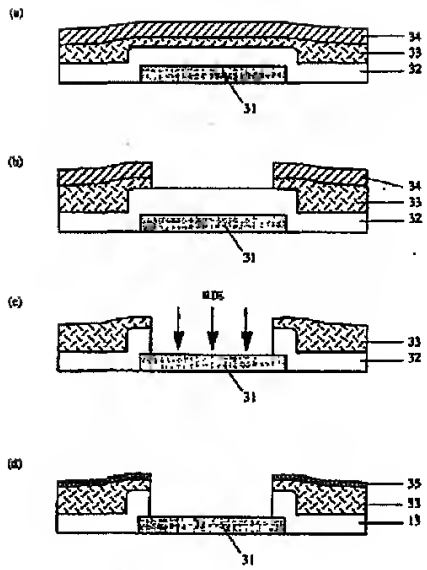

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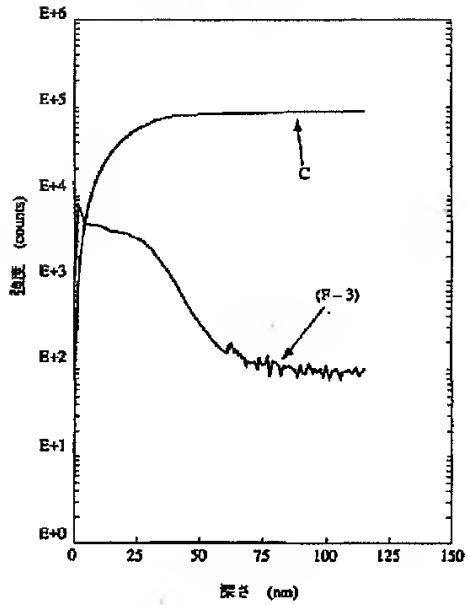

フロントページの続き

(51) Int. Cl.[6]	識別記号	庁内整理番号	FI	技術表示箇所
H01L 21/312		B 7352－4M		
21/3213				
		8826－4M	H01L 21/88	D

(19) Japan Patent Office (JP)

(12) Publication of Patent Application (A)

(11) Japanese Published Patent Application No. H7-58107

(43) Date of Publication: March 3, 1995

(51) Int. Cl.[6] Identification Symbol FI

H01L	21/3205				
	21/3065	M	7352-4M		
	21/312		8826-4M	H01L 21/88	T
				21/302	N

Request for Examination: Not made

Number of Claims: 2 OL (5 pages in total) *Continued on the last page*

(21) Japanese Patent Application No. H5-203810

(22) Application Date: August 18, 1993

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(54) [Title of the Invention]

MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

(57) [Summary]

[Structure]

A process of forming a laminated passivation film including a polyimide film 13 and an inorganic insulating film 12 includes a step of removing a certain amount of a surface layer of the polyimide film 13 after forming a laminated passivation film by a step of forming the inorganic insulating film 12 for passivation over a metal wiring 11 having a predetermined pattern over a semiconductor substrate and by a step of forming the polyimide film 13, and after forming an opening in the laminated passivation film at a predetermined position by a step of opening the polyimide film 13 and a step of opening the inorganic insulating film 12 with the polyimide film 13 used as a mask.

[Effect]

According to a manufacturing method of a semiconductor device of the present invention, a manufacturing method of a semiconductor device can be provided in which adhesion with the molding resin is good and the corrosion of pads and wirings is not easily caused even if moisture intrudes into a molding resin.

[Scope of Claims]

[Claim 1]

A manufacturing method of a semiconductor device comprising a step of forming a laminated passivation film having a step of forming an inorganic insulating film over a metal wiring formed over a semiconductor substrate; a step of forming a polyimide film over the inorganic insulating film; a step of forming a photoresist over the polyimide film; a step of providing a predetermined opening in the polyimide film by etching with the photoresist which had been formed into a predetermined shape used as a mask; a step of removing the photoresist; a step of subjecting the inorganic insulating film to dry etching by RIE with the polyimide film used as a mask; and a step of removing a certain amount of a surface layer of the polyimide film.

[Claim 2]

The manufacturing method of a semiconductor device according to claim 1, wherein the step of removing the certain amount of the surface layer of the polyimide film is performed by an O_2 plasma asher method.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to a semiconductor device and a manufacturing method thereof, particularly, a step of forming an opening in an inorganic insulating film layer in a laminated passivation film including a polyimide film and the inorganic insulating film layer.

[0002]

[Prior Art]

An example of a conventional step of processing an opening in a laminated passivation film including a polyimide film and an inorganic insulating film layer is described with reference to FIGS. 3 and 4. First, an inorganic insulating film 32 and a polyimide film 33 which is subjected to only low-temperature baking are sequentially formed over a metal wiring 31 having a predetermined pattern which is formed over a semiconductor substrate, and then, the polyimide film 33 is coated with a positive type photoresist 34 (FIG. 3(a)). Subsequently, light exposure and development are performed, and the polyimide film 33 is etched concurrently with development of the positive type photoresist 34 to provide a predetermined opening in the polyimide film 33 (FIG. 3(b)). After the positive type photoresist 34 is selectively separated using an organic solvent, predetermined heat treatment is performed to imidize the polyimide film 33. Next, after the inorganic insulating film 32 is opened by a general reactive ion etching (hereinafter, abbreviated as RIE) with the polyimide film 33 used as a mask (FIG. 3(c)), washing by water and polyimide reheat treatment are performed, so that the formation of an opening in a laminated passivation film including a polyimide film and an inorganic insulating film is completed (FIG. 3(d)).

[0003]

As described above, in a conventional method for forming an opening in a laminated passivation film of a polyimide film and an inorganic insulating film, at the time of processing an opening, the inorganic insulating film is opened by a dry etching method such as RIE with the polyimide film used as a mask. Dry etching is a method in which a reactive gas is injected in vacuum so that etching is performed by chemical reaction. In general, for dry etching of a silicon oxide film (including a film doped

with an impurity), a silicon nitride film, or the like, gas including a fluorine element is used. General chemical equations in this case are given below. It is to be noted that F^* refers to fluorine in a radical state which is extremely and chemically active.

[0004]

$SiO_2+F^* \rightarrow SiF_4+O_2$

$Si_3N_4+F^* \rightarrow SiF_4+N_2$

However, this etching gas produces an unsaturated monomer in plasma, and under the influence of this etching residue, a high-concentration fluorine remaining layer 35 is formed in a surface layer of the polyimide film as shown in FIG. 3(d).

[0005]

FIG. 4 shows the concentration of each element in a polyimide film in a conventional example as depth profiling. The horizontal axis indicates a depth in the polyimide film, and the vertical axis indicates the concentration of each element. As shown in a graph (F-3), the concentration of fluorine is extremely high in the vicinity of the surface. The high-concentration fluorine remaining layer 35 is hardly removed in a subsequent treatment by a reheat treatment (350°C - 60 minutes). Owing to such a high-concentration fluorine remaining layer 35, the following problems occur.

[0006]

First, due to reaction by contact with moisture in the atmospheric air after etching or reaction between moisture intruding into a molding resin and fluorine in a fluorine remaining layer, hydrofluoric acid is formed, and thus, the corrosion of wirings is caused by the corrosion of pad portions or the like. The corrosion of wirings not only reduces yield of elements but also shortens the reliability life of the wirings and causes shortening of the life of elements. The reliability life according to a pressure and cooker test (high-temperature and high-pressure steam test, which is one of items for reliability assessment and hereinafter abbreviated as PCT) is 80 hours ~ 150 hours, which is short. Further, variation is widened.

[0007]

Second, adhesion with a molding resin is weakened by the existence of the fluorine remaining layer. According to a temperature cycling test (one of items for

reliability assessment, and hereinafter, abbreviated as TCT), separation from the mold occurs at 200 ~ 400 cycles. This makes moisture easy to intrude from outside, and due to this, occurrence of a problem or the like of the corrosion of wirings which is caused by the formation of hydrofluoric acid, is promoted. Accordingly, the level of reliability is further reduced.

[0008]

[Problems to be Solved by the Invention]

As described above, a conventional manufacturing method of a semiconductor device has problems as follows: the high-concentration fluorine remaining layer is formed in the surface layer of the polyimide film by fluorine containing gas used for dry etching in forming an opening in the laminated passivation film including the polyimide film and the inorganic insulating film. Under the influence of this, after sealing with a molding resin is performed, the corrosion of wirings of a pad portion or the like is caused, and further, separation from the molding resin occurs, which leads to reduction in reliability.

[0009]

In order to solve the above-described problems, it is an object of the present invention to provide a semiconductor device with increased reliability accomplished by almost complete removal of fluorine remaining in a polyimide film surface after dry etching, and a manufacturing method of the semiconductor device.

[0010]

[Means for Solving the Problem]

In order to solve the above-described objects, the present invention provides a manufacturing method of a semiconductor device which includes a step of forming a laminated passivation film which has a step of forming an inorganic insulating film over a metal wiring formed over a semiconductor substrate, a step of forming a polyimide film over the inorganic insulating film, a step of forming a photoresist over the polyimide film, a step of providing a predetermined opening in the polyimide film by etching with the photoresist which had been formed into a predetermined shape used as a mask, a step of removing the photoresist, a step of subjecting the inorganic insulating

film to dry etching by RIE with the polyimide film used as a mask, and a step of removing a certain amount of a surface layer of the polyimide film. Further, the present invention provides the manufacturing method of a semiconductor device where the step of removing the certain amount of the surface layer of the polyimide film is performed by an O_2 plasma asher method.

[0011]

[Operation]

According to the semiconductor device and the manufacturing method of the semiconductor device of the present invention which is structured as described above, by almost complete removal of fluorine remaining in a polyimide film surface after dry etching, the corrosion of pads or poor adhesion with a molding resin can be suppressed, and accordingly, reliability can be improved.

[0012]

[Embodiment]

One embodiment of the present invention is described with reference to FIGS. 1 and 2. FIGS. 1(a) to 1(e) are cross-sectional views showing a manufacturing process of a semiconductor device in one embodiment of the present invention. Hereinafter, a manufacturing process of this embodiment is described.

[0013]

First, over a metal wiring 11 (thickness: approximately 1.0 μm) which has a predetermined pattern and is formed from, for example, Al-Si, a P-SiO film having a thickness of 1 μm is formed as an inorganic insulating film 12 by a general plasma CVD method. The P-SiO film, which is the inorganic insulating film 12, is coated with a polyimide film 13 to a thickness of approximately 3.2 μm (4000 rpm - 60 seconds), and further, after baking at 140 °C (5 minutes), the polyimide film 13 is coated with a positive type photoresist 14 to a thickness of approximately 2.5 μm (4000 rpm - 30 seconds) and baking is performed at 110 °C (60 seconds) (FIG. 1(a)).

[0014]

Light exposure is performed using a mask having a predetermined pattern, and then, development of the positive type photoresist 14 and etching of the polyimide film

13 are successively performed using an alkaline-based developing solution, so that a predetermined pattern is formed in the polyimide film 13 (see FIG. 1(b)).

[0015]

Subsequently, the positive type photoresist 14 is selectively removed using an organic solvent, and then, baking is performed using a predetermined procedure ((250 °C - 30 minutes) + (350 °C - 40 minutes)), so that imidization of the polyimide film 13 is completed. After that, the inorganic insulating film 12 is opened by dry etching by general RIE with the polyimide film 13 having a predetermined opening used as a mask (FIG. 1(c)).

[0016]

Further, after removing approximately 2000 angstrom of the surface layer of the polyimide film 13 by an O_2 plasma asher method, which is performed as processing of the polyimide surface layer which had been subjected to dry etching, that is, a fluorine remaining layer 15 (FIG. 1(d)), washing by water (10 minutes) and heat treatment (350 °C - 60 minutes) are performed, so that a laminated passivation film is completed which includes the polyimide film 13 and the inorganic insulating film 12 without the fluorine remaining layer 15 in the polyimide film 13 (FIG. 1(e)).

[0017]

In this embodiment, an O_2 plasma asher method is performed as processing of the fluorine remaining layer in the polyimide surface layer. However, there may be no limitation to an O_2 plasma asher method as long as a chemical etching method is used in which fluorine is not adsorbed again. Further, as the amount of removing the polyimide surface layer, 2,000 angstrom thereof is removed. However, of course, there is no problem in that the amount of removal is equal to or less than that as long as the fluorine remaining layer can be completely removed. Accordingly, for example, at least 800 angstrom or more thereof is likely to be removed in consideration of the result of analysis in this embodiment. The amount of removing the polyimide surface layer may be decided in accordance with the targeted laminated passivation film or conditions. Furthermore, there is no problem that the P-SiO film used as the inorganic insulating film and other constituent materials are formed from other materials as long as they are

suitable. The photoresist is not necessarily a positive type photoresist, and a suitable one is used in accordance with the case.

[0018]

FIGS. 2(a) and (b) show the concentration of each element in a polyimide film as depth profiling. The horizontal axis indicates a depth in the polyimide film, and the vertical axis indicates the concentration of each element. A graph (F-1) in FIG. 2(a) shows depth profiling of fluorine remaining in a polyimide film which has been subjected to processing of a surface layer of the polyimide film. A graph (F-2) in FIG. 2(b) shows depth profiling of fluorine in a sample which is not subjected to dry etching after the formation of a laminated passivation film. For example, in the case where 2000 angstrom of the surface is removed by an O_2 plasma asher method as in the above-described embodiment, fluorine is hardly detected as shown in FIG. 2(a) in a similar manner to the sample in FIG. 2(b) which is not subjected to dry etching such as RIE.

[0019]

As above, when an O_2 plasma asher method as described above is performed, almost complete removal of a fluorine remaining layer in a polyimide surface is possible. Therefore, the following are provided as advantages. First, since there is no fluorine, the corrosion of pads and wirings does not easily occur even if moisture intrudes into a molding resin. For example, the reliability life of 400 or more hours can be obtained according to a PCT, which are 2.6 ~ 5 times longer than the conventional reliability life.

[0020]

Further, adhesion with a molding resin is stable since a fluorine remaining layer does not exist. Thus, separation from the mold does not occur in a TCT even when the cycles reach 1000. Accordingly, a semiconductor device with increased reliability can be obtained into which moisture does not easily intrude from outside.

[0021]

[Effect of the Invention]

According to a manufacturing method of a semiconductor device using the

present invention, a manufacturing method of a semiconductor device can be provided in which adhesion with a molding resin is good and the corrosion of pads and wirings does not easily occur even if moisture intrudes into the molding resin.

[Brief Description of the Drawings]

[FIG. 1] (a) to (e) are cross-sectional views showing a manufacturing process in one embodiment of the present invention.

[FIG. 2] (a) is a drawing which shows depth application of fluorine remaining in a polyimide film after processing of the surface layer of the polyimide film, and (b) is a view showing depth profiling of fluorine in a sample which is not subjected to dry etching after formation of a laminated passivation film.

[FIG. 3] (a) to (d) are cross-sectional views showing a manufacturing process in a conventional example.

[FIG. 4] A drawing which shows depth profiling of fluorine remaining in a polyimide film after dry etching.

[Explanation of Reference]

11: metal wiring 12: inorganic insulating film 13: polyimide film 14: positive type photoresist 15: fluorine remaining layer

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(51) Int. Cl.[6]	Identification Symbol	JPO file Number	FI	
H01L 21/312		B 7352-4M		
21/3213				
		8826-4M	H01L 21/88	D

Section showing technique